SBC3005 Intel Tiger Lake UP3 Single Board Computer

High-Performance DO-254 Certifiable SBC IP

FEATURES AND BENEFITS

- 3U VITA 65 OpenVPX™ plug-in card based on the 11th Gen Intel® Core™ processor
    - 4-core 1.8 GHz (4.4 GHz) 15 W Intel i7-1185GRE processor
    - 16 GB dual channel DDR4 memory controllers with ECC
    - PCIe Gen 3 data plane and expansion plane on the VPX fabric connector
- XMC site supporting 1 x 8 Gen 3 PCIe and X12d + 16s + X8d rear I/O
- Part of the COTS-D family of safety certifiable modules
- Rugged conduction-cooled module - 3U SOSA-aligned VITA 65 (OpenVPX) solution
    - SOSA 3U I/O intensive module profile: SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16, MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15–2
- A complete hardware solution with data package to support certification to RTCA DO-254/EUROCAE ED-80
- Board Support Packages (BSP) available, as well as data packages to support certification to RTCA DO-178C/ EUROCAE ED-12C
- The provision of all IP and data to enable manufacture, support, and repair of the module
- Board Safety Monitor including temperature, voltage, clocks, and watchdog.
- Operating card edge temperature range of –40 to +85°C
- 3U VPX powered from +12 V, +3.3 V Aux, and VBAT

INTRODUCTION

The SBC3005 11th Gen Intel Tiger Lake Single Board Computer (SBC) is ideal for avionics and defense applications looking for next generation processing. The SBC3005 provides a safety certifiable multi-core processor including an XMC expansion site to maximize the functionality in a single slot of a 3U VPX system. The SBC complements the GPMX002 graphics mezzanine with an eight lane PCIe Gen 3 interface for high-performance graphics and compute.
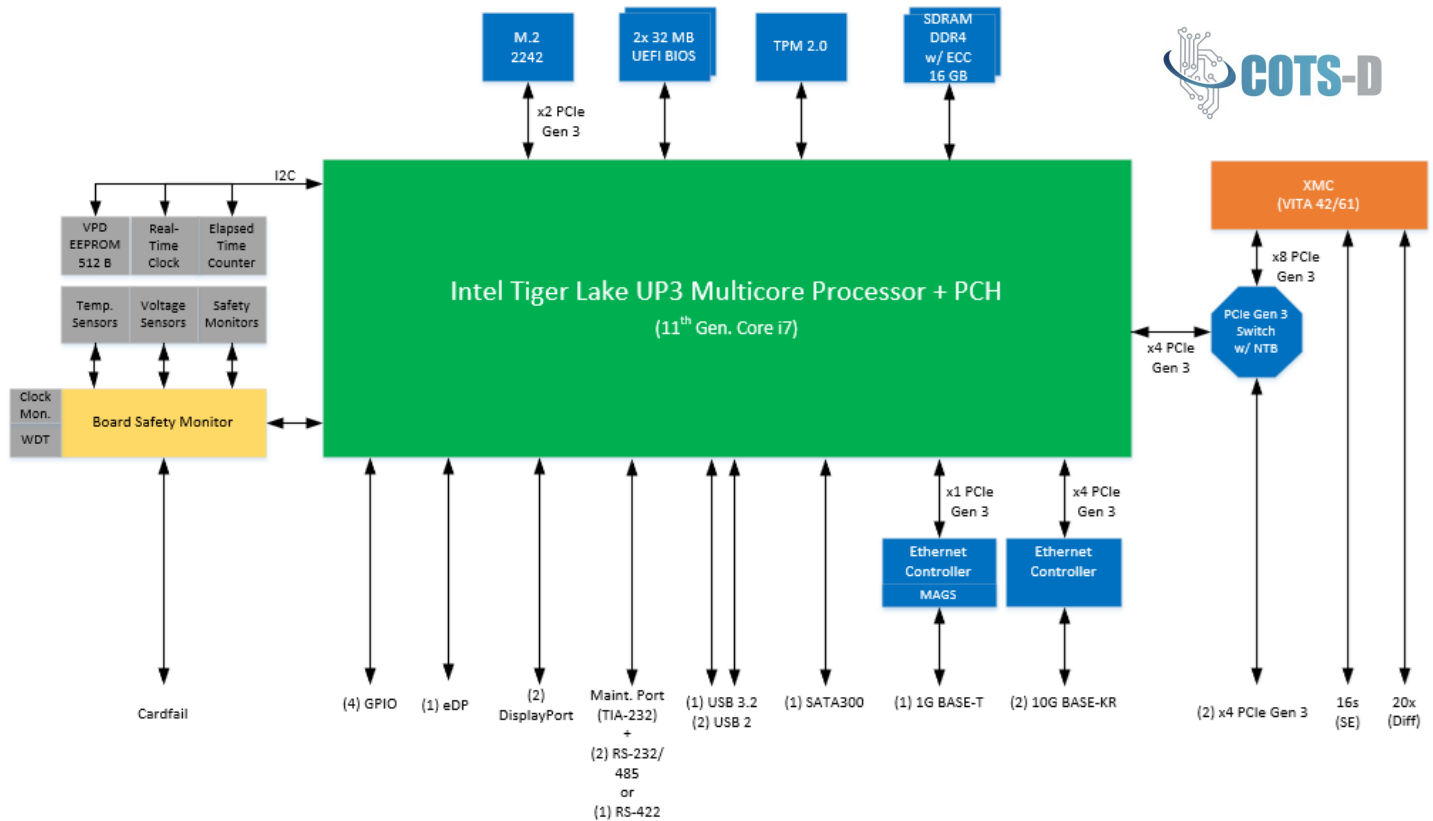
Figure 1: SBC3005 Intel Tiger Lake UP3 Block Diagram

PROCESSING

The Intel Tiger Lake UP3 system-on-chip (SoC) (SKU i7-1185GREC-RT) is the next generation in application processors from Intel that is targeted toward the embedded rugged Mil/Aero/Avionics and Industrial markets. The Tiger Lake UP3 offers a high degree of functional integration for advanced multi-display systems with low virtualization software overhead.

The Tiger Lake UP3 SoC is comprised of four CPU cores along with an integrated Iris® X^e graphics processing unit. This high level of integrated processing, graphics, and connectivity makes it a very compact, power efficient solution ideal for embedded applications and for use on space-constrained modules.

The Tiger Lake SoC is particularly well suited to mission and safety-critical applications. Any and all "commercial" features that pose challenges to deterministic operations (like thermal auto-throttle) can be disabled.

Figure 2: SBC3005 Intel Tiger Lake UP3 COTS-D SBC

MEMORY

The following table summarizes available memory.

MEMORY	SIZE	TYPICAL USE
DDR4 ECC DRAM	16 GB	Main Application Memory In-Band ECC Dual Channel Architecture
SPI Flash	32 MB x 2	BIOS
Mass Storage	M.2 SSD Site	2230 or 2242 Module Form Factor x2 PCIe Interface Write Protect NVMe Device Interface

Table 1: Available Memory

INPUTS AND OUTPUTS

The following table summarizes the available input and output interfaces.

INTERFACE	QUANTITY	TYPICAL USE
Serial	2 x RS232, or 1 x RS422, or 2 x RS485 half-duplex	Accessed via P2 1 x Maintenance Port accessed via P1
Ethernet	1 x 1000BASE-T 2 x 10GBASE-KR	10/100/1000BASE-T Ethernet via P2 with Magnetics 10GBASE-KR via P1 (VITA 46.7) Supports IEEE 1588 PTP
GPIO	4	
PCIe	2 x 4 lane PCIe Gen 3	Data Plane and Expansion Plane via P1 support two non-transparent ports Support for backplane common clock option
SATA	1 x SATA300	Accessed via P2
USB	1 x USB 3.2 2 x USB 2.0	Accessed via P2
Video	2 x Display Port v1.2 1 x eDP	Resolutions up to 3850 x 2160 @ 60 Hz Supports audio and video via P2
XMC	1 x X12d + 16s + X8d	Up to Gen 3 PCIe, VITA 61 XMC 2.0 Connector VPWR + 12 V

Table 2: Available Inputs and Outputs

LOCAL FUNCTIONS

The SBC3005 includes an Elapsed Time Counter (ETC) to track module up-time to assist with maintenance activities, and a Real Time Clock (RTC) for 1 pulse per second (PPS) timing synchronization related requirements.

EXPANSION

Within a 3U VPX system, the capabilities of the module can be expanded. The processor may be configured to have two x4 PCIe Gen 3 communication/data links with up to two independent modules.

Local card expansion is supported by a standard XMC 2.0 (VITA 61) expansion interface powered by +12 V VPWR with an 8-lane PCIe Gen 3 interface. The Pn6 I/O is mapped per SOSA 3U I/O Intensive SBC module -2 profile (VITA 46.9 P1W9-X12D, P2 X16S, P2 X8D) to the backplane. VITA 61 is based on the VITA 42 XMC replacing the connectors with alternative footprint-compatible, ruggedized, high-speed mezzanine interconnectors. VITA 61 is pin compatible with the VITA 42 standard; therefore, it supports VITA 42 as a build option. The XMC site supports industry standard XMC modules including the CoreAVI GPMX002 E9171 COTS-D Graphics Processor Module, which is available to provide high-performance graphics capability.

SAFETY AND SECURITY FEATURES

The SBC3005 uses CoreAVI's DAL A Certified Board Safety Monitor FPGA to support safety, built-in test (BIT) and card health monitoring requirements. The safety monitors include temperature, voltage, and clock. Two temperature monitors monitoring module temperature are under application control, while voltage and clock out-of-range would result in the module being shut down. The safety monitor FPGA performs Power-On BIT (PBIT) and Continuous BIT evaluation for a fault condition, a failure of any of the monitors, or a software failure indicator, and will assert a CardFail signal to the backplane. In addition to the monitors, there is an independent watch dog timer that will time out and cause a module reset if not kicked by the application before timing out.

The SBC3005 also features a Trusted Platform Module (TPM 2.0).

ELECTRICAL SPECIFICATIONS

The SBC3005 is designed to run from the +12 V rails and +3.3 V auxiliary with maximum typical current as set out in the following table, based on the execution of a representative application at the highest rated operating temperature.

VOLTAGE	TYPICAL CURRENT (AMPS)
+12 V (VS1)	3.00
+5 V (VS2)	Not connected
+3.3 V (VS3)	Not connected
+12 V Auxiliary	Routed to XMC site
-12 V Auxiliary	Routed to XMC site
+3.3 V Auxiliary	0.3

Table 3: Maximum Typical Current

MECHANICAL SPECIFICATIONS

The mechanical specifications are set out in the following table.

CHARACTERISTIC	SPECIFICATION
3U VPX form-factor (VITA 46.0, VITA 48.0)	3.9 inches x 6.3 inches (100 mm x 160 mm)
Slot Width	1.0 inch VPX-REDI Type 1, RCR-Series Type 1 Extended Covers Two Level Maintenance (VITA 48.2)
Backplane Connectors	VITA 46.0
XMC Connectors	VITA 61

Table 4: Mechanical Specifications

ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are set out in the following table.

ENVIRONMENT	SPECIFICATION
Operating Temperature	-40 to +85°C
Storage Temperature	-55 to +105°C
Vibration	0.1g²/Hz Random
Shock	40 g
Humidity	5% to 95% Relative Non-Condensing Humidity
Altitude	-1,500 to 60,000 feet (-460 to 18,300 meters)

Table 5: Environmental Specifications

TIGER LAKE UP3 SOC LONG-TERM SUPPLY AND SUPPORT

CoreAVI provides consistent and dedicated support for the supply and use of the Intel Tiger Lake UP3 SoC within the rugged Mil/Aero/Avionics market segments. CoreAVI will ensure that the software, hardware, and long-life support are provided to meet the needs of customers' system life cycles.

CoreAVI has extensive environmentally controlled storage facilities that are used to store the SoCs supplied to the Mil/Aero/Avionics marketplace, ensuring that a ready supply is available for the duration of any program.

CoreAVI also provides the post Last Time Buy storage of SoCs and is often able to provide additional quantities of components when COTS hardware partners receive increased volume for existing products/systems requiring additional inventory.

EVALUATION SUPPORT

CoreAVI provides lab development hardware for all its COTS-D Hardware IP designs to enable customers to get started early on platform development. To support customers in the development of their Tiger Lake-based applications, CoreAVI offers a standard commercial Tiger Lake UP3 development board, compatible with an industry standard PCIe interface.

VkCore® SC drivers as well as VkCoreGL® SC1, VkCoreGL® SC2, ComputeCore™ and VkCoreVX™ SC application libraries are available for Windows 10 and Linux. These products are available on a 12-month evaluation license that includes support. Please refer to these products' respective product briefs for more detailed product information.

COTS-D DATA KIT

The COTS-D Data Kit provides all the data to enable support, manufacture, and repair of the SBC3005. Key elements of the data package include:

- Manufacturing data
- Theory of Operations
- Bill of Materials including full manufacturers part numbers
- Schematics
- PLD design files
- Mechanical drawings and assembly diagrams
- Printed Circuit Board (PCB) drawings and data

Please request the COTS-D application note, which provides further details on the data items and support provided for the technical transfer. The technical transfer also includes training and support as you introduce the product to your manufacturing facility or that of your chosen contract manufacturer.

DO-178C/ED-12C DATA KIT

The DO-178C/ED-12C Data Kit provides documentation and evidence for the SBC3005 to support FAA and EASA certification needs of the hardware elements, as well as PLDs to support Item Development Assurance Level (IDAL) A.

ORDERING

The following SBC3005 products can be ordered from CoreAVI:

- SBC3005-C000 SBC module for development purposes: conduction-cooled
- SBC3005-0020 COTS-D Design/Manufacturing Data Kit & license to use
- SBC3005-001x Safety Critical Data Kit supporting DO-254/ED-80
- RTM3005-1000 Rear Transition Module (RTM) for development purposes (see below)

REAR TRANSITION MODULE

An RTM (RTM3005-1000) that plugs into the backside of the backplane in the same slot as the SBC3005 is available. The RTM provides access to the I/O using industry standard connectors as set out in the following table.

RTM3005-1000 INPUTS AND OUTPUTS	
Front panel accesses 1 x DisplayPort 1 x 1000BASE-T (RJ45) 1 x USB 3.0 1 x USB 2.0 1 x RS232 Maint (RJ45)	**Internal accesses** 4 x GPIO 2 x RS232/1 x RS422 - XMC I/O (X12d + Xd + X16s) - Battery

Table 6: RTM3005-1000 I/O

Contact Sales@CoreAVI.com to discuss your requirements and obtain a quote.